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A Multicore SDR Architecture for Reconfigurable WiMAX Downlink

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Abstract—This paper describes a multicore Software Defined Radio (SDR) architecture devised to implement a fully reconfigurable downlink for WiMAX transceivers. The proposed architecture is made up of Commercial-Off-The-Shelf (COTS) modules available in the market and includes a DSP, three different models of FPGAs, DACs and ADCs. We show that the architecture is capable of supporting all the functionalities of the downlink subframe of the Orthogonal Frequency Division Multiple Access (OFDMA) WiMAX physical layer, including Partial Usage of Subcarriers (PUSC) symbol structure and Forward Error Correction (FEC). The primary advantage of the design is the full reconfigurability at different levels: bandwidth, size of the FFT, modulation, code rate, etc. without modifying or restarting the system. We show that the five downlink profiles defined by the WiMAX Forum can be successfully implemented with the proposed architecture.

Index Terms—WiMAX; SDR; FPGA; OFDMA; prototype;

I. INTRODUCTION

WiMAX is a Broadband Wireless Access (BWA) technology that enables ubiquitous delivery of wireless broadband services to either fixed and/or mobile services [1]. It is a technology based on the IEEE 802.16 standard for the delivery of last-mile wireless broadband access and it has been proposed as an alternative to cable and DSL. The name WiMAX was coined by the WiMAX Forum which was formed to promote conformity and interoperability of the standard [2].

There are two basic amendments for the IEEE 802.16 standard: the 802.16-2004 [3], also referred to as “fixed WiMAX”, and the 802.16e [4] that introduced support for mobility and for that reason is known as “mobile WiMAX”. Most commercial interest is nowadays in 802.16e because it supports mobility and uses lower frequencies that experience less propagation attenuation and exhibit better in-building penetration.

The physical (PHY) layer of a WiMAX transceiver is basically made up of an inner Orthogonal Frequency Division Multiple Access (OFDMA) modulator/demodulator and an outer Forward Error Correction (FEC) encoder/decoder. OFDMA is an extension of the OFDM modulation which allows several users to simultaneously access the medium.

The various functionalities present in a WiMAX transceiver have different technical requirements and duty cycles. Thus, it is more appropriate to implement the transceiver on a multicore Software Defined Radio (SDR) hardware architecture where each core is adapted to a specific functionality. This is much more efficient than attempting to implement the whole system on a single very flexible core [5].

The proposed multicore SDR architecture is based on Commercial-Off-The-Shelf (COTS) modules available in the market. In our case, we use COTS hardware made up of a PCI carrier board with several TIMs (Texas Instruments Module). Basically, we have four different module types: a DSP, three different FPGAs, DACs and ADCs. We will show in this work that these hardware elements provide enough processing power to implement a fully reconfigurable downlink of the WiMAX PHY layer provided an appropriate distribution of the tasks among the processing elements is carefully chosen.

This paper is structured as follows. Section II presents a brief description of the WiMAX PHY layer downlink. In Section III we describe the multicore SDR hardware architecture. In Section IV we describe the design methodology to successfully implement a fully-reconfigurable WiMAX PHY layer downlink. Section V presents the results from the experimental evaluation of the constructed prototype and, finally, Section VI is devoted to the conclusions.

II. WiMAX PHYSICAL LAYER

A frame in the OFDMA PHY layer is made up of a downlink subframe from the base station to the mobile stations, and an uplink subframe. The downlink subframe is composed of one OFDM symbol for the preamble and a series of OFDM symbols with a defined structure of pilots and data. The 802.16e standard defines several structures where Partial Usage of Subcarriers (PUSC) and Full Usage of Subcarriers (FUSC) are the two most prominent examples.

There are several FEC encoding methods supported by the WiMAX PHY layer —e.g. Convolutional Coding (CC), Convolutional Turbo-Coding (CTC), Block Turbo-Coding (BTC) and Low Density Parity Check (LDPC). Each burst can be
encoded using any of these techniques. In addition, the standard supports a variable code rate and modulation to enable Adaptive Modulation and Coding (AMC) capabilities.

The bursts are mapped into the OFDM symbols defining rectangular regions in time and frequency domains. We have focused on the only mandatory channel encoding method, which is convolutional encoding with tail-biting. In this case, the code rates are 1/2, 3/4 and, additionally, 2/3 when 64-QAM is used.

In addition, there are requirements at the profile level. WiMAX Forum defines profiles with different bandwidths and number of subcarriers (see Table I). The size of the cyclic prefix can be also variable, with sizes ranging from 1/4 to 1/32 of the symbol length.

In summary, we have focused on the mandatory sections of the downlink subframe: PUSC zone with support for several bursts, OFDM modulation and convolutional coding.

III. Multicore Hardware Architecture

The selected hardware is based on COTS signal processing modules. The PCI carrier board can include up to four TIMs. The first module occupies two TIMs, and contains a Texas Instruments TMS320C6416 DSP together with a Xilinx Virtex-II XC2V6000 FPGA. This FPGA is well suited for logic operations and data transfers. The second module contains an FPGA Xilinx Virtex-4 XC4SX55. The third module contains a FPGA Xilinx Virtex-4 XC4VSX35 and an analog add-on module that contains two DACs and two ADCs. Both Xilinx Virtex-4 XC4SX55 and Xilinx Virtex-4 XC4VSX35 FPGAs are equipped with a large number of embedded multipliers enabling intensive signal processing operations. The same configuration is used for the transmitter and the receiver.

For the communications between modules there are two different types of buses: control buses, with a throughput of 20 MB/s, that are used for configuration messages; and data buses, with a throughput of 400 MB/s, that are used for data exchange between modules.

IV. Prototype Design

The main advantage of the previously described hardware architecture is its flexibility, enabling to meet the requirements of both signal processing operations and high-level control logic demanded by the distinct elements of the software design. The kernel of the architecture is constituted by the DSP. It is responsible of executing the higher-level tasks, which requires the highest degree of freedom and the most complex operations, as well as controlling the executions in the remaining elements of the system (mainly the tasks running in the different FPGAs).

The hardware architecture also contains several FPGAs providing the processing power demanded by the 802.16e standard. The main drawback, among the disadvantages of using FPGAs, is the implementation difficulty of the tasks that require real-time reconfigurability capabilities. Because of this, it is preferable to view the FPGAs as coprocessors of the DSP.

Having in mind the previously described practical constraints, the methodology that we have followed is the following:

1) Identify the time-consuming tasks that will be placed on the FPGAs. A good design should minimize the number of these tasks.
2) Decouple the tasks among them to minimize the propagation of the modifications introduced in the tasks due to the reconfigurability needs.
3) Minimize the degree of reconfigurability present on every task.
4) Use the task template shown in Fig. 1. This template defines the structure of a task, which is made up of two different paths: one for the data —including the processing steps— and another one for the configuration.

The main advantage of the proposed reconfigurable architecture, together with the implementation methodology, is that the entire design can be divided in easier to implement tasks thanks to the architecture flexibility (each task is placed on the DSP or on a FPGA according to its duty cycle requirements) and the template for the tasks.

A. Implementation

Fig. 2 shows the partition of the modem functionalities, and which core they have been implemented in. First of all, the host sends to the MAC_CTRL task inside the DSP the transmission parameters and then it sends or receives the data from the MAC_CTRL block. This block creates bursts according to a predefined configuration that can be changed in each transmission. In the current implementation, the bursts are created with the maximum size allowed by the number of symbols in the frame, the modulation and the code rate. Since the MAC layer is not implemented, these parameters are sent before the beginning of a transmission is started, and are known for both the transmitter and the receiver.

The bursts are sent to the task PHY_CTRL, which encodes and maps the information to QAM symbols using the FEC block, and sends the data to the PUSC block. For our tests, only one burst is transmitted in each frame. The PHY_CTRL block is also the responsible of sending configuration registers to the first block in each processing chain.

The PUSC block deals with the subchannelization of data carriers, pilots and guard insertion. This process depends on the size of the FFT, and the task can be reconfigured to change
this size dynamically, calculating the new symbol structure from the parameters defined in the standard.

Next, the frame built by the PUSC block is sent to the OFDM block. The first one is the IFFT/FFT which can be configured with either 512 or 1024 FFT sizes, and different cyclic prefix sizes. The Frame generation task is responsible of sending frames with the time constraints defined in the standard.

The last task at the OFDM transmitter is the Digital Up Converter (DUC), which filters and upconverts the baseband samples to an arbitrary intermediate frequency. The pulse-shaping should be capable to generate the following bandwidths defined by the WiMAX Forum: 4 MHz, 5.6 MHz, 8 MHz, 10 MHz, and 11.2 MHz. These baseband bandwidths generate the profiles shown in Table I, taking into account the guard bands.

In order to minimize the resources used in the FPGA, there is a filter bank whose interconnections should be properly chosen according to the desired bandwidth. The different configurations of this filter bank are shown in Fig. 4, where all baseband signals are interpolated to 80 MHz (DAC sampling frequency). It is apparent from this figure that some of the interpolation/decimation filters can be reused in the implementation of the different profiles. Indeed, the filter bank can be built on the basis of five filters with upsampling and downsampling factors: 7, 5, 4, and 2. The use of interpolating and downsampling filters yields to an efficient implementation in terms of consumed resources with reduced multiplier usage.

At the receiver, there is an additional task: the Synchronization block. This block performs frame and symbol detection using the correlation properties of the preamble and the OFDM symbols. It also carries out a frequency offset estimation and correction. The algorithms implemented in this part of the system are a correlation of the cyclic prefix with the end of the OFDM symbol, and a correlation of the second third of the symbol with the last third to detect a preamble [6]. The phase of this correlations is used to estimate the frequency offset.

The FEC layer is made up of a randomizer, an interleaver, and a convolutional encoder at the transmitter; and a Viterbi decoder at the receiver. The block is capable of dividing the input data into blocks according to the rules described in the 802.16e standard. The mapping and the demapping operations are also done inside the FEC layer, and the supported modulations are 4-QAM, 16-QAM and 64-QAM. The demapper returns soft-bits from the carriers extracted from the OFDM symbols.

V. Results
In order to evaluate the constructed 802.16e fully reconfigurable downlink transceiver prototype, we have measured the
TABLE II
EVM LEVELS FOR DIFFERENT PROFILES

<table>
<thead>
<tr>
<th></th>
<th>3.5 MHz</th>
<th>5 MHz</th>
<th>7 MHz</th>
<th>8.75 MHz</th>
<th>10 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td>-40.70 dB</td>
<td>-37.88 dB</td>
<td>-40.83 dB</td>
<td>-40.70 dB</td>
<td>-37.42 dB</td>
</tr>
<tr>
<td>RF</td>
<td>-35.81 dB</td>
<td>-34.66 dB</td>
<td>-34.59 dB</td>
<td>-34.03 dB</td>
<td>-33.50 dB</td>
</tr>
</tbody>
</table>

EVM (Error Vector Magnitude) of the received carriers.

In the host, a test application was implemented to check the prototype performance. The transmitter can generate random data, or obtain it from a file, and the receiver can acquire the symbols of a number of frames and calculate the EVM. It can also decode the received bits and compare them with those in the transmitted file to estimate the Bit Error Ratio (BER).

We performed tests over two different scenarios: intermediate frequency (IF) transmission through a cable, and radio-frequency (RF) transmission with antennas at a distance of 2 m. The carrier frequency of the IF tests was set at 15 MHz. The RF tests were carried out using the Agilent VSG E4438C signal generator as upconverter and the ACSC-RX-5255 downconverter, built by the Spanish company Acorde Technologies. The carrier frequency used for these tests was 5.255 GHz.

Table II shows the EVM values obtained for the five profiles defined by the WiMAX Forum from the IF and the RF experiments. The EVM was calculated from 100 frames made up of two OFDM symbols each, transmitted with a power value equal to -10 dBm. The excellent performance exhibited by the constructed prototype is apparent from the results at IF: EVM values are smaller than -37 dB in all cases. Moreover, in the 3.5 MHz, 7 MHz, and 8.75 MHz profiles the EVM is smaller than -40 dB. There is a performance degradation of about 3 dB in the 5 MHz and the 10 MHz but this is because the filter banks are in this case made up of four cascaded interpolation/decimation stages instead of only two, as in the other profiles.

Finally, the received 64-QAM constellations for the 8.75 MHz and the 10 MHz profiles are shown in Fig. 5 and Fig. 6. They correspond to EVM values of -34.0 dB, and -33.5 dB, respectively. The excellent performance achieved with the reconfigurable prototype is apparent from the high quality of the constellations.

VI. CONCLUSION

In this paper, we have presented a multicore Software Defined Radio (SDR) hardware architecture suitable for the implementation of a fully reconfigurable WiMAX PHY layer downlink. The proposed multicore SDR architecture is made up of Commercial-Off-The-Shelf (COTS) modules available in the market. It includes a DSP, three different models of FPGAs, DACs, and ADCs. We have explained a methodology that has been followed to successfully assign modem functionalities to the different hardware modules. Finally, we presented the results of a prototype implementation, and showed minimum differences (less than 3 dB in terms of EVM) between the five profiles defined by the WiMAX Forum.